

Undergraduate Programme in Physics

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MODULE HANDBOOK

Module Name	Digital Electronics													
Module level, if applicable	Bachelor													
Code, if applicable	FIS414011													
Subtitle, if applicable	-													
Courses, if applicable	Digital Electronics (Elektronika Digital)													
Semester(s) in which the module is taught	3 rd (Third)													
Person responsible for the module	Chair of Instrumentation Interest Area													
Lecturer(s)	Nia Maharani, S.T., M.Eng.													
Language	Indonesia													
Relation to curriculum	Compulsary course in the second year (3 rd semester) Bachelor Degree													
Type of teaching, contact hours	150 minutes lectures and 180 minutes structured activities per week.													
Workload	Total workload is 136 hours per semester, which consists of 150 minutes lectures per week for 14 weeks, 180 minutes structured activities per week, 180 minutes individual study per week, in total is 16 weeks per semester, including mid exam and final exam													
Credit points	3													
Requirements according to the examination regulations	Minimum attendance 75% All assignments must be submitted before the exam													
Recommended prerequisites	No prerequisites stated on													
Module objectives/intended learning outcomes	<p>After completing this course, the students:</p> <ul style="list-style-type: none"> CO 1. Understand the number system in digital electronics and its conversion from one number to another CO 2. Understand and apply combinational logic circuits: NOT, AND, OR, XOR, NAND, and NOR CO 3. Understand and apply latch and flip-flop CO 4. Understand and apply binary counters CO 5. Understand and apply shift register CO 6. Understand digital electronics-based technology 													
Content	<ul style="list-style-type: none"> a. Number systems: decimal, binary, hexadecimal, octal, BCD, and ASCII code. b. Conversion from one number to another number. c. Combinational logic circuits: NOT, AND, OR, XOR, NAND, NOR. d. Sequential logic circuits: latches and flip-flops, binary counters, shift registers. 													
Study and examination requirements and forms of examination	<p>The final mark will be weighted as follows:</p> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 5%;">NO</th> <th style="width: 75%;">Assessment methods (components, activities)</th> <th style="width: 20%;">Weight (percentage)</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>Final Examination</td> <td>35%</td> </tr> <tr> <td>2</td> <td>Mid-Term Examination</td> <td>35%</td> </tr> <tr> <td>3</td> <td>Class Activities : Quiz, Homework, etc.</td> <td>30%</td> </tr> </tbody> </table>		NO	Assessment methods (components, activities)	Weight (percentage)	1	Final Examination	35%	2	Mid-Term Examination	35%	3	Class Activities : Quiz, Homework, etc.	30%
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	<p>The final assessment is expressed in the form of a letter value converted from a number value with the following categories:</p> <table border="1"> <thead> <tr> <th>NO</th> <th>Number Value</th> <th>Letter Value</th> <th>NO</th> <th>Number Value</th> <th>Letter Value</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>≥ 95</td> <td>A</td> <td>7</td> <td>65-69.99</td> <td>B/C</td> </tr> <tr> <td>2</td> <td>90-94.99</td> <td>A-</td> <td>8</td> <td>60-64.99</td> <td>C+</td> </tr> <tr> <td>3</td> <td>85-89.99</td> <td>A/B</td> <td>9</td> <td>55-59.99</td> <td>C</td> </tr> <tr> <td>4</td> <td>80-84.99</td> <td>B+</td> <td>10</td> <td>50-54.99</td> <td>C-</td> </tr> <tr> <td>5</td> <td>75-79.99</td> <td>B</td> <td>11</td> <td>55-34.99</td> <td>D</td> </tr> <tr> <td>6</td> <td>70-74.99</td> <td>B-</td> <td>12</td> <td><35</td> <td>E</td> </tr> </tbody> </table>	NO	Number Value	Letter Value	NO	Number Value	Letter Value	1	≥ 95	A	7	65-69.99	B/C	2	90-94.99	A-	8	60-64.99	C+	3	85-89.99	A/B	9	55-59.99	C	4	80-84.99	B+	10	50-54.99	C-	5	75-79.99	B	11	55-34.99	D	6	70-74.99	B-	12	<35	E
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Media employed	White-board, Lcd Projector, e-learning (https://daring.uin-suka.ac.id/)																																										
Reading list	<ol style="list-style-type: none"> 1. Tertulien Ndjountche . 2016. <i>Digital Electronics 1: Combinational Logic Circuits</i>. ISTE Ltd and John Willey & Sons, Inc. 2. Tertulien Ndjountche . 2016. <i>Digital Electronics 2: Sequential and Arithmetic Logic Circuits</i>. ISTE Ltd and John Willey & Sons, Inc. 3. John Crowe and Barrie Hayes-Gill. 1998. <i>Introduction to Digital Electronics</i>. Newnes. 																																										

PLO and CO Mapping

	PLO 1	PLO 2	PLO 3	PLO 4	PLO 5	PLO 6	PLO 7	PLO 8	PLO 9
CO 1			√						
CO 2			√	√	√				
CO 3			√	√	√				
CO 4			√	√	√				
CO 5			√	√	√				
CO 6			√						